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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/685,655	10/14/2003	Sung-Jin Kim	8750-038	5662
20575	7590	06/05/2006	EXAMINER	
MARGER JOHNSON & MCCOLLOM, P.C. 210 SW MORRISON STREET, SUITE 400 PORTLAND, OR 97204				VU. HUNG K
ART UNIT		PAPER NUMBER		
		2811		

DATE MAILED: 06/05/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/685,655	KIM ET AL.
	Examiner Hung Vu	Art Unit 2811

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 14 March 2006.
- 2a) This action is FINAL. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 7-20 and 23-34 is/are pending in the application.
- 4a) Of the above claim(s) 7-11,17-20,24 and 28-32 is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 12-16,23,25-27,33 and 34 is/are rejected.
- 7) Claim(s) _____ is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date: _____ |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>3/14/06</u> | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Request for Continued Examination

1 A request for continued examination (RCE) under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicants' submission filed on 03/14/06 has been entered. An action on the RCE follows.

Election/Restrictions

2. Newly submitted claims 24 and 28-32 are directed to an invention that is independent or distinct from the invention originally claimed for the following reasons: Claims 24 and 28-32 are not belong to the elected embodiment of Figure 5B. Note that Figure 5B does not show a vertical plane running along the length of the third upper interconnection line and the fourth upper interconnection line bisects the third upper interconnection line and the further upper interconnection line.

Since applicant has received an action on the merits for the originally presented invention, this invention has been constructively elected by original presentation for prosecution on the merits. Accordingly, claims 24 and 28-32 are withdrawn from consideration as being directed to a non-elected invention. See 37 CFR 1.142(b) and MPEP § 821.03.

Claim Objections

3. Claim 12 is objected to because of the following informalities:

In claim 12, lines 14-15, “and and” should be changed to “and” for clarity.

In claim 12, line 16, after “a third upper interconnection”, insert --line-- for clarity.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 12-16, 23, 25-27 and 33-34 are rejected under 35 U.S.C. 102(b) as being anticipated by Noguchi et al. (US 2001/0017418, of record).
Noguchi et al. discloses, as shown in Figures 1-5 and 15, a semiconductor device having multi-layered interconnection lines, the semiconductor device comprising:

lower interconnection lines (1) disposed on a semiconductor substrate (10), the lower interconnection lines substantially coplanar, the lower interconnection lines aligned in a first direction and disposed parallel to one another, the lower interconnection lines including a first lower interconnection line, a second lower interconnection line, and a third lower interconnection line between the first and second lower interconnection lines, an end of the first lower interconnection line and an end of the second lower interconnection line disposed a substantially

equal distance away from an end of the third lower interconnection line [see Fig. 4, a third, a fourth and a fifth (1) from the left of Figure 4];

an interlayer insulating layer (13) disposed on a surface of the substrate having the lower interconnection lines;

upper interconnection lines (3) disposed on the insulating layer, the upper interconnection lines substantially coplanar, the upper interconnection lines aligned in the first direction and disposed parallel to each other, the upper interconnection lines including a first upper interconnection line, a second upper interconnection line, and a third upper interconnection line (3) [see Fig. 4, the first, second, and third lines (3) from the right of Figure 4]

Regarding claim 13, Noguchi et al. discloses the device further comprising: a fourth upper interconnection line (3) formed on the insulating layer and located on the same line as the third upper interconnection line but separated from it by a distance, the distance between the third and fourth upper interconnection lines being greater than a longest focus distance [note that since the upper surface of the interlayer dielectric layer 13 and/or interconnection line 3 is planar, the focus should be zero].

Regarding claims 14 and 25, Noguchi et al. discloses the lower interconnection lines comprise a layer chosen from the group consisting of poly-silicon layer, a silicide layer and a metal layer [0088].

Regarding claims 15 and 26, Noguchi et al. discloses the interlayer insulating layer comprises at least one layer selected from the group consisting of BPSG, USG, PSG, SOG and PE-TEOS [0086] (note that USG and TEOS are silicon oxide).

Also note that the term “PE” is method recitation in a device claimed. “[E]ven though product-by-process claims are limited by and defined by the process, determination of patentability is based on the product itself. The patentability of a product does not depend on its method of production. If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product was made by a different process.” *In re Thorpe*, 777 F.2d 695, 698, 227 USPQ 964, 966 (Fed. Cir. 1985)..

Regarding claims 16 and 27, Noguchi et al. discloses the upper interconnection lines comprise a layer chosen from the group consisting of poly-silicon layer, a silicide layer and a metal layer [0088].

Regarding claim 23, Noguchi et al. discloses, as shown in Figures 1-5 and 15, a semiconductor device comprising:

lower interconnection lines (1) or (4), the lower interconnection lines substantially coplanar and disposed parallel to each other on a semiconductor substrate (10), the lower interconnection lines including a first lower interconnection line, a second lower interconnection line, and a third lower interconnection line between the first and second lower interconnection lines, the first and second lower interconnection lines extending past an end of the third lower

interconnection line [see Fig. 4, a third, a fourth and a fifth (1) from the left of Figure 4 or a third, a fourth and a fifth (4) from the bottom of Figure 4];

an interlayer insulating layer (13) formed on an entire surface of the substrate having the lower interconnection lines;

upper interconnection lines (3) or (2), the upper interconnection lines substantially coplanar and disposed parallel to each other on the insulating layer, the upper interconnection lines disposed parallel to and aligned in the same direction as the lower interconnection lines, the upper interconnection lines including a first upper interconnection line, a second upper interconnection line, and a third upper interconnection line between the first and second upper interconnection lines [see Figs. 4 and 5].

Regarding claim 33, Noguchi et al. discloses the upper interconnection lines (3) and the lower interconnection lines (1) are disposed such that a vertical projection of each of the first upper interconnection line, second upper interconnection line and third interconnection line on upper surface of the first lower interconnection line, second lower interconnection line, and third lower interconnection line, respectively, lies within the boundaries defined by the upper surfaces of the first lower interconnection line, the second lower interconnection line, and the third lower interconnection, respectively [see Figure 4].

Regarding claim 34, Noguchi et al. discloses the lengths of the upper interconnection lines (3) and the lengths of the lower interconnection lines (1) are aligned in the same direction.

Response to Arguments

5. Applicant's arguments filed 03/14/06 have been fully considered but they are not persuasive.

It is argued, at page 8 of the Remarks, that Figure 5B discloses the first lower interconnection line and the first upper interconnection line are aligned such that a first vertical plane running lengthwise to the first lower and upper interconnection lines bisect both of them. This argument is not convincing because Figure 5B does not show the claimed invention.

It is argued, at page 9 of the Remarks, that Figures 4 and 5 of Noguchi et al. does not disclose the upper interconnection line align in the same direction as the lower interconnection lines. This argument is not convincing because Noguchi et al. discloses, as shown in Figure 4, the upper interconnection line (3) align in the same direction as the lower interconnection lines (1).

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hung Vu whose telephone number is (571) 272-1666. The examiner can normally be reached on Tuesday to Friday 6:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C. Lee can be reached on (571) 272 - 1732. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Vu

May 15, 2006

Hung Vu
Hung Vu

Primary Examiner